## **IN THE CLAIMS:**

1. (Previously presented) An error detection system for a clock signal comprising: 1 2 a first counter that receives and counts the clock signal, a phase-locked loop circuit that receives the clock signal and outputs a second 3 clock signal, 4 a second counter that receives and counts the second clock signal, 5 a comparator that receives and compares the outputs of the first and the second 6 counters, and 7 an error output from the comparator that is true when the counts of the first and 8 second counters are unequal. 9 2. (Previously presented) The error detection system as defined in claim 1 further 1 comprising a second output from the comparator that indicates which counter contains a 2 higher count. 3 3. (Original) The error detection system as defined in claim 1 further comprising ı 2 means for resetting the counters synchronized to the successful capture of the clock signal by the PLL. 3 4. (Previously presented) The error detection system as defined in claim 1 further 1 comprising: 2

a sender that sends data and the clock signal, the clock signal defined as a for-3 warding source synchronous clock signal, and 4 a receiver latch that accepts and latches the data therein with the forwarding 5 clock. 5 (Original) A method for detecting clock signal errors comprising the steps of: 1 a first counting of the first clock signals, 2 providing a second clock signal with a frequency that is locked to the average fre-3 quency of the first clock signal, a second counting of the second clock signals, 5 detecting a difference between the first and the second countings, and 6 signaling an error therewith. 7 6. (Original) The method as defined in claim 5 further comprising the step of: signalling which counting is higher. 2 7 (Previously presented) The method as defined in claim 5 further comprising the 1 step of synchronizing the two countings. 2 8. (Original) The method as defined in claim 5 further comprising the steps of: 1 sending data and the clock signal, wherein the clock signal is a forwarding source 2 synchronous clock signal, 3

receiving the data, and 4 latching the data with the forwarding clock signal. 5 9. (Previously presented) A system for detecting errors in a first clock signal, the 1 system comprising: means for counting the first clock signal, 3 means, responsive to the first clock signal, for generating a second clock signal, 5 means for counting the second clock signal, means for comparing the count of the first clock signal with the count of the sec-6 ond clock signal, and 7 means for generating an error when the count of the first clock signal differs from 8 the count of the second clock signal. 9 10. (Previously presented) The system of claim 9 wherein the first clock signal has an average frequency, and 2 the second clock signal is locked to the average frequency of the first clock signal. 3 11. (Previously presented) The system of claim 9 wherein 1 the first clock signal has a plurality of rising edges and a plurality of falling edges, 2 and 3 the means for counting the first clock signal counts one of the rising and falling 4

edges.

5

12. (Previously presented) The system of claim 9 wherein 1 2 the first clock signal has a plurality of rising edges and a plurality of falling edges. and 3 the means for counting the first clock signal counts both the rising and falling edges. 13. (Previously presented) The system of claim 10 wherein the means for generating a second clock signal includes a phase lock loop (PLL) circuit. 2 1 14. (Previously presented) The system of claim 9 further comprising means for determining whether the count of the first clock signal is higher or lower than the count 2 of the second clock signal. 3 15. (New) The system of claim 14 wherein the means for generating a second 1 clock signal includes a phase lock loop (PLL) circuit. 2 16. (New) The system of claim 14 wherein the first clock signal has an average frequency, and 2

the second clock signal is locked to the average frequency of the first clock signal.

3